

IN THE CLAIMS:

✓ Please cancel Claims 1-19 without prejudice or disclaimer of the subject matter presented therein.

✓ Please add new Claims 20-29 as follows.

1-19 (Cancelled)

20. (New) An image pickup element comprising:

a pixel area including a plurality of partial pixel-areas, wherein said plurality of partial pixel-areas are arranged two-dimensionally in horizontal and vertical directions, and wherein each of said plurality of partial pixel-areas include photodetectors arranged two-dimensionally in the horizontal and vertical directions;

a vertical-direction selecting circuit which selects, in common, photodetectors arranged in the horizontal direction on a plurality of horizontal lines basis from among the photodetectors arranged two-dimensionally;

a horizontal-direction selecting circuit which selects, in common, photodetectors arranged in the vertical direction on a plurality of vertical lines basis from among the photodetectors arranged two-dimensionally; and

a plurality of output lines which output, in parallel, signals from the photodetectors selected by said vertical-direction selecting circuit and said horizontal-direction selecting circuit,

wherein said vertical-direction selecting circuit and said horizontal-direction selecting circuit are controlled so that said plurality of output lines output the signals of the selected photodetectors on a partial pixel-area basis.

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21. (New) An image pickup element according to claim 20, wherein said pixel area includes a color filter array so that each of said plurality of partial pixel-areas includes a color filter of a Bayer array.

22. (New) An image pickup element according to claim 20, wherein said pixel area includes a four-complementary-color filter array arranged on a partial pixel-area basis.

23. (New) An image pickup element formed on a single semiconductor chip, comprising:

a pixel area including an arrangement of a plurality of blocks, each block including at least two photo-detection elements;

a plurality of output lines which output, in parallel, signals from said at least two photo-detection elements of the block; and

an operation section which inputs, in parallel, the signals outputted in parallel from said plurality of output lines, wherein said operation section performs an interpolation processing to interpolate a predetermined signal using signals other than the predetermined signal.

a) 24. (New) An image pickup element according to claim 23, wherein said pixel area includes a plurality of partial pixel-areas arranged two-dimensionally in horizontal and vertical directions, and wherein each of said plurality of partial pixel-areas includes photodetectors arranged two-dimensionally in the horizontal and vertical directions,

B said image pickup element further comprising a memory which stores signals of a plurality of lines of the photodetectors arranged in the horizontal direction, and a selecting circuit which reads out the signals in parallel from said memory to said plurality of output lines on a partial pixel-area basis.

25. (New) An image pickup element formed on a single semiconductor chip, comprising:

a pixel area including an arrangement of a plurality of blocks, each block including at least two photo-detection elements;

a plurality of output lines which output, in parallel, signals from said at least two photo-detection elements of the block; and

an operation section which inputs, in parallel, the signals outputted in parallel from said plurality of output lines, wherein said operation section performs a compression processing.

26. (New) An image pickup element according to claim 25, wherein said pixel area includes a plurality of partial pixel-areas arranged two-dimensionally in horizontal and vertical directions, and wherein each of said plurality of partial pixel-areas includes photodetectors arranged two-dimensionally in the horizontal and vertical directions,

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said image pickup element further comprising a memory which stores signals of a plurality of lines of the photodetectors arranged in the horizontal direction, and a selecting circuit which reads out the signals in parallel from said memory to said plurality of output lines on a partial pixel-area basis.

27. (New) An image pickup element according to claim 25, wherein the compression processing includes a discrete cosine transform.

28. (New) An image pickup element formed on a single semiconductor chip, comprising:

a pixel area including an arrangement of a plurality of blocks, each block including at least two photo-detection elements;

a plurality of output lines which output, in parallel, signals from said at least two photo-detection elements of the block; and

an operation section which inputs, in parallel, the signals outputted in parallel from said plurality of output lines, wherein said operation section performs an edge emphasis processing.

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29. (New) An image pickup element according to claim 28, wherein said pixel area includes a plurality of partial pixel-areas arranged two-dimensionally in horizontal and vertical directions, and wherein each of said plurality of partial pixel-areas includes photodetectors arranged two-dimensionally in the horizontal and vertical directions,

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said image pickup element further comprising a memory which stores signals of a plurality of lines of the photodetectors arranged in the horizontal direction, and a selecting circuit which reads out the signals, in parallel, from said memory to said plurality of output lines on a partial pixel-area basis.